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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,257	03/19/2001	Lowell E. Kolb	10001844-1	2624

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,257	KOLB ET AL.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The request filed on 01/24/05 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/813,257 is acceptable and a RCE has been established. An action on the RCE follows.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1, 3-5, 7, 11-12, 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by McCullough et al. (U. S. Patent 6,127,038), in the record.

As to claim 1, McCullough et al. disclose a printed circuit board (PCB, 12-figure 1, column 2, line 37) comprising:

a printed wiring board (PWB); a component (22, column 3, line 1) mounted on said PWB, wherein the PWB has a volume of space bounded by at least one of a body of the component (22), a lead (24, column 3, line 2) of the component, and the printed wiring board, wherein the volume of space has at least one opening on the surface of the PWB; (***note***: it should be noted that the space would defined as a space on top and bottom surface of the PWB, a space that is formed underneath of the leads of the

component, or as a space that formed between each of the components 22 mounted on the PWB 12); and

an electrically non-conductive filler material (14, column 3, lines 8, 52-64) disposed on the surface of the PWB so as bridge across the at least one opening of the volume space to render the volume of space substantially *inaccessible to* subsequently-applied coatings (16, column 3, line 15).

As to claim 12, McCullough et al. disclose a printed circuit board (PCB, 12-figure 1, column 2, line 37) comprising:

a printed wiring board (PWB); a plurality of components (22, column 3, line 1), each mounted on said PWB, wherein the printed circuit board has at least one volume of space (*see the note in claim* 1) bounded by at least one component lead (24), a component body (a body of a component 22), and the printed wiring board (PWB), wherein each at least one volume of space comprises at least one opening (underneath of component 22 or between the components) on the surface of the PCB; and

a layer of non-electrically-conductive filler material (14, column 3, lines 8, 52-64) adhered to the PCB surface to provide a contoured, contiguous filler material surface, wherein the filler material at least partially infill the at least one volume of space through the at least one opening and further wherein the filler material bridge across the at least one space so as to encapsulate and seal the volume of space (top and bottom surfaces of the PWB, underneath of leads of the component, or space between the components).

As to claim 3, McCullough et al. disclose the space comprises the space is bounded by leads (24), of the body of components (22) and the PWB, wherein at least

one of the at least one space/openings on the surface of the PCB is located between neighboring component leads (24).

As to claim 4, McCullough et al. disclose the component is one of a plurality of components (22), and wherein the space is bounded by at least two or more of the plurality of components or between the components (22) and the PCB.

As to claim 5, McCullough et al. discloses the space bounded by the component (22) and the PWB.

As to claims 7 and 14, McCullough et al. disclose the filler material is an epoxy (column 3, lines 52-54).

As to claim 11, McCullough discloses the subsequently-applied coating (16) comprises a layer of dielectric coating (see column 3, lines 65-66) that conformingly coats exposed surfaces of the PWB, the component (22), and the filler material (14), wherein the at least one opening of the space is sufficiently large to prevent the dielectric coating from bridging across the opening without the presence of the filler material.

As to claim 15, McCullough et al disclose the PCB further comprising a low viscosity, high adherence dielectric coating (16) that, when applied and cured, covers portions of said PCB coated with sad filler material (14), wherein the filler material (14) prevents the dielectric coating (16) from entering the at least one space.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 8-10, 13, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCullough et al. (U. S. Patent 6,127,038) in view of Kotani et al. (JP 200034457 A, hereafter JP), in the record.

As to claim 6, 9, 13, and 17, McCullough et al. do not disclose all of the limitations of the claimed invention; except for the filler material is thixotropic, or thermally cured epoxy.

Kotani et al. (JP) shows a high-pressure resistant thixotropic epoxy resin adhesive (see abstract), the adhesive includies a thermally cured epoxy.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ thixotropic epoxy resin including a thermally cured epoxy in the PCB of McCullough, as taught by Kotani et al. (JP) for the purpose of retaining a sufficient adhesion thickness under high bearing pressure and maintaining a strength at high temperature that applied on the surface of the PCB.

As to claim 8, McCullough et al. do not disclose said epoxy is one of the family of Bisphenol-A epoxies mixed with an amine hardener.

Kotani et al. (JP) shows a epoxy resin is one of the family of Bisphenaol-A epoxies mixed with an amine hardener (see pages 2-3 of the translation).

It would have been obvious to one of ordinary skill in the art at the invention was made to employ a epoxy resin is one of the family of Bisphenaol-A epoxies mixed with an amine harder in the PCB of McCullough, as taught by Kotani et al. for purpose of providing a stiffness and high temperature performance.

As to claim 10, McCullough et al. do not disclose said epoxy be a latex based non-electrically conductive epoxy. Kotani et al. shows a epoxy resin that is a latex based non-electrically conductive composition (see pages 2-3 of the translation).

It would have been obvious to one of ordinary skill in the art at the invention was made to employ a epoxy resin is a latex based non-electrically conductive epoxy in the PCB of McCullough, as taught by Kotani et al. for purpose of providing a high resistance to damage from moisture and high temperature performance.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCullough et al. (U. S. Patent 6,127,038) in view of Higgins, III (U. S. Patent 5,639,989), in the record.

As to claim 16, McCullough et al. do not disclose the PCB further comprising a conductive coating covered at least a portion of the dielectric coating layer, and the conductive and dielectric coatings are formed a conformal electromagnetic interface (EMI) shield that adheres to and conforms with the PCB surfaces.

Higgins, III shows a conductive coating (62) covered a dielectric coating layer (60-figure 3), and the conductive and dielectric coatings are formed a conformal

electromagnetic interface (EMI) shield that adheres to and conforms with the PCB surfaces, see column 9, lines 53-67.

It would have been obvious to one of ordinary skill in the art at the invention was made to employ a conductive coating covered a dielectric coating in the PCB of McCullough, as taught by Higgins, III, for purpose of providing ground shielding potential to the PCB.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 3-17 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues:

Applicant argues a first coating layer (14) in the McCullough that does not bridging across an opening of the volume of space on the PCB as recited in claims 1 and 12.

Examiner disagrees. McCullough clearly discloses in figure 1 that the first coating layer (14) does bridging across an opening of the volume of space because the space would defined as: a space on a top or a bottom surface of the PWB (12), a space that is formed underneath of the leads of the component see figure 1, or as a space that formed between each of the components 22 mounted on the PWB 12. Therefore, examiner believes the Office action is proper and including all of the limitations of the claimed languages.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
March 01, 2005.